IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Adkisson et al.
Serial No. 09/691,353 Group Art Unit 2823
Filed October 18, 2000 Examiner K. Nguyen
For METHOD OF FABRICATING SEMICONDUCTOR SIDE WALL FIN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.132
OF
JAMES W. ADKISSON

Sir:

JAMES W. ADKISSON declares as follows:

1. I received a B.S. in Physics from MIT, with a Masters and PhD from Stanford University, where I worked on hetero-epitaxial growth of GaAs on Si for optoelectronic applications.

2. I am employed by International Business Machines Corporation at their Microelectronics facility in Burlington, Vermont, where I am a senior engineer. I have worked at IBM for thirteen years in semiconductor technology.

3. I have reviewed the subject patent application, including the claims, and the examiner's remarks as contained in the Office Action mailed on September 7, 2004. I have also reviewed the U.S. Patent Publication No. 2003/0006410 to Brian Doyle.

4. With specific regard to the Doyle patent publication, Doyle is using Sidewall Image Transfer (SIT) to mask narrow channels in the silicon. That

is, his channels are all below the surface of the original oxide steps (item 14 in Figs 1 and 2). To do this, he deposits nitride layers (item 16) as etch mask layers in Figs 1b and 2b.

5. The nitride layers (item 16) are amorphous dielectric layers. These amorphous depositions lack the crystalline properties of epitaxial depositions.

6. The technical meaning of "epitaxial" is very specific and precludes the use of amorphous dielectric layers. A definition from Semiconductor Glossary (attached) is as follows, although any materials science text or reference would use the same definition:

> epitaxy: process by which thin layer of single-crystal material is deposited on single-crystal substrate; epitaxial growth occurs in such way that the crystallographic structure of the substrate is reproduced in the growing material; also crystalline defects of the substrate are reproduced in the growing material.

7. We have limited our claims to use only epitaxial growth for a number of reasons. First, we want the carrier transport channels to be nearly perfect for optimum electron transport. The purpose of this method is to allow band-gap tailoring of the channel (for optimum charged-carrier transport) and well-controlled widths for the channels; epitaxy is a good method to do this. To remove them (as Doyle removes his nitride layers) would defeat the idea of the present invention.

8. Doyle does not perform epitaxial growth, and in fact teaches away from the use of epitaxial growth by describing nitride layers, which are amorphous dielectrics and not semiconductor crystals. The use of epitaxy, as in the definition above, assumes a crystalline layer which is perfectly, or essentially perfectly, aligned to the original material, which is itself a crystalline material.

9. In addition, Doyle's layers are used as sacrificial etch masks, whereas the layers we grow epitaxially are used as the conductive channels. Doyle's layers are neither present after the process is complete, nor could they be since they are not effective conductors.

10. Further, what the examiner points to in his review of claim 15 as semiconductor lines (item 14, in Fig. 2a of Doyle), which are necessary to form a crystalline template, are in fact oxide lines. By definition, these oxide lines are amorphous, without crystalline structure. Therefore, it makes no sense to compare them to the semiconductor lines referred to in claim 15. They clearly are not the single crystal substrate required for epitaxial growth.

11. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above referenced application and any patent issuing thereon.

Date: Nov. 8, 2004

JAMES W. ADKISSON